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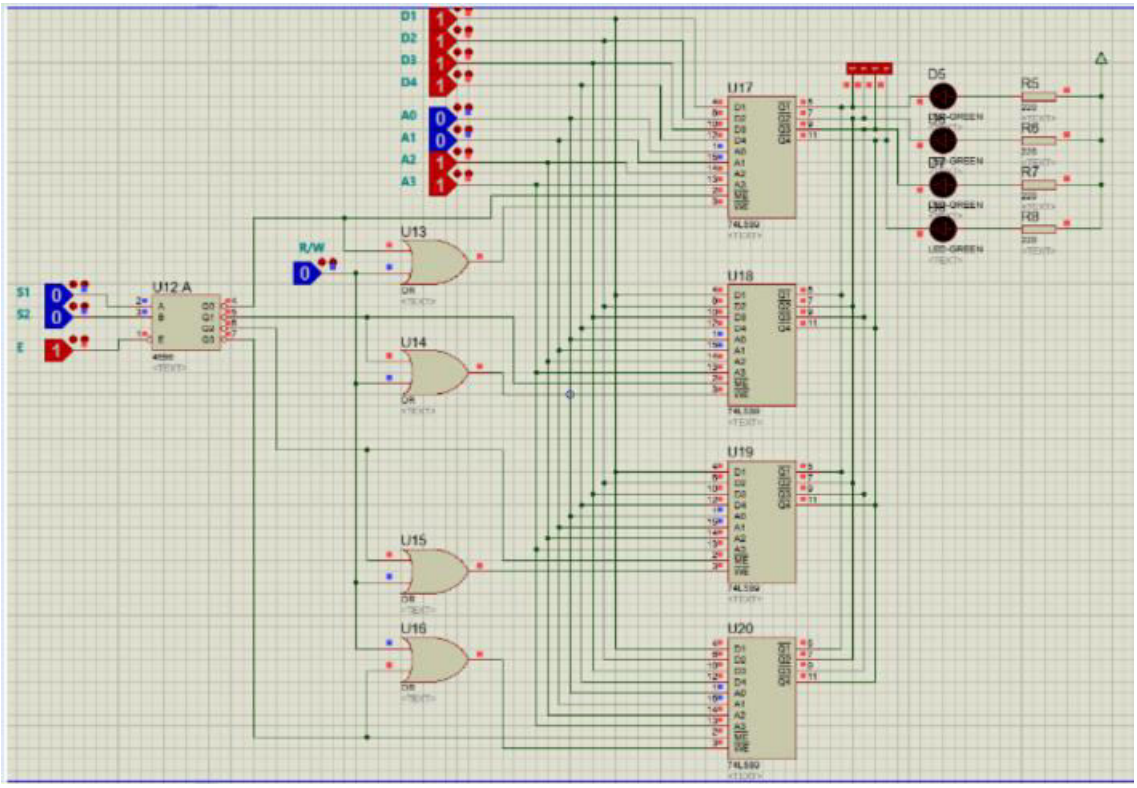
post lab 7

1) Design a 4x16 RAM using four 4x4 RAMS.



First, we need to design four separate 4x4 RAMs. Each RAM will have 4 address lines, A0-A3, four data lines, D0-D3, and an active low write line (WR*).

The four 4x4 RAMs then need to be connected together to form a single 4x16 RAM. The four RAMs can be connected in parallel. To do this, the four address lines A0-A3 from each RAM will be connected together, and the four data lines D0-D3 from each RAM will be connected together. The WR* lines from each RAM will be connected together and will act as a single active low write line for the 4x16 RAM.

The 4x16 RAM is now complete. It will have 4 address lines, A0-A3, sixteen data lines, D0-D15, and an active low write line, WR*.

2) Although D latches are useful for storing binary information, they are not used in RAM circuit

design, why?

D latches are not used in RAM circuit design because they are not capable of providing the quick access time required for RAM. D latches also have limited output stability, which is not suitable for RAM.