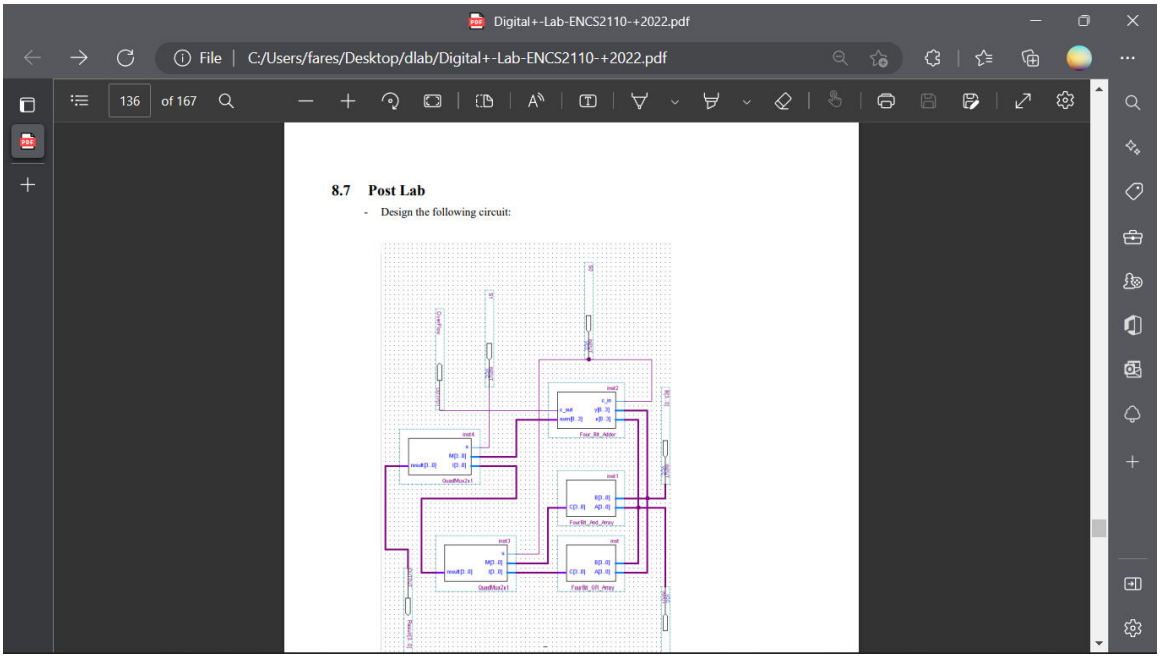
Name:: Asmaa abed Al-Rahman Fares

Std.No::1210084

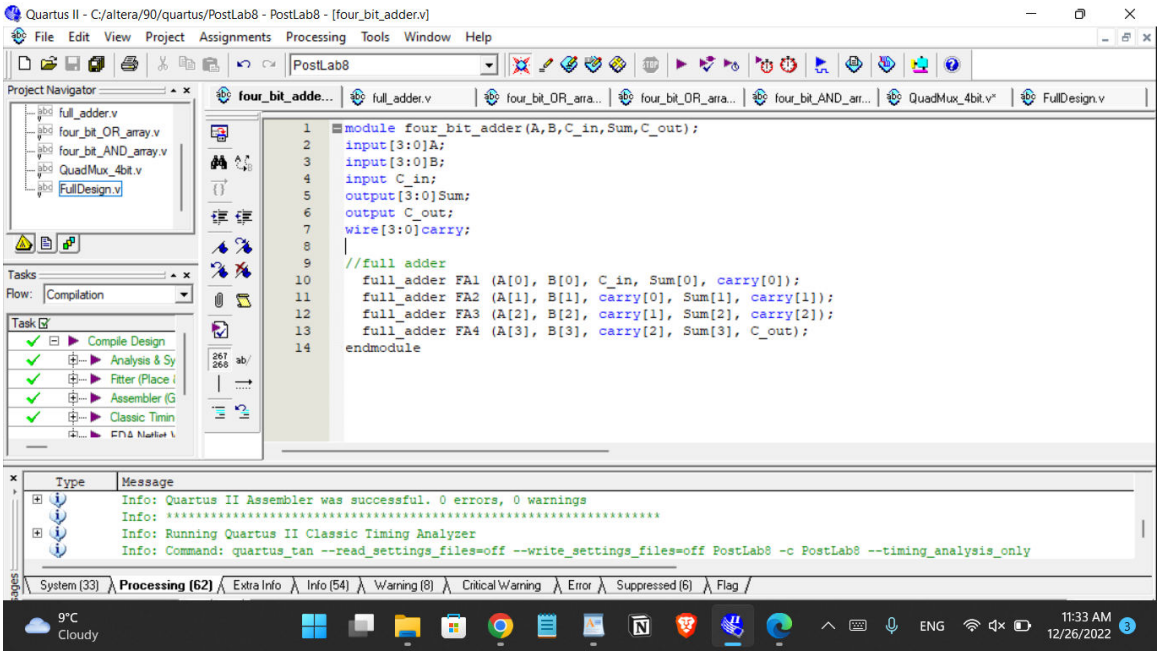
section 1

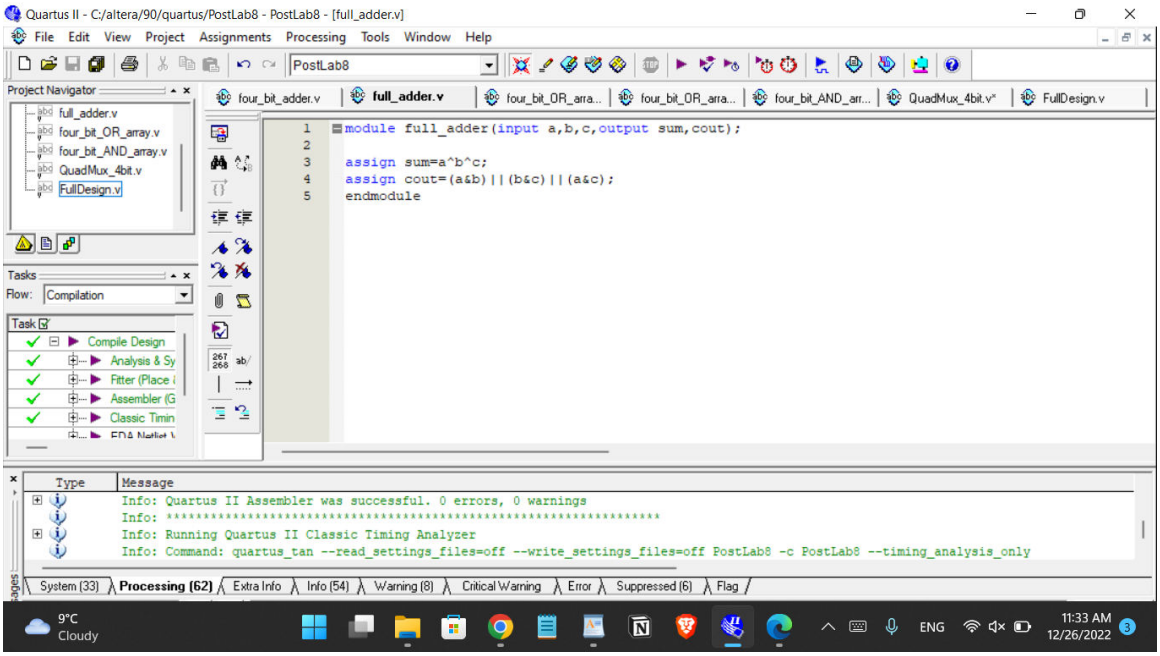
PostLab8

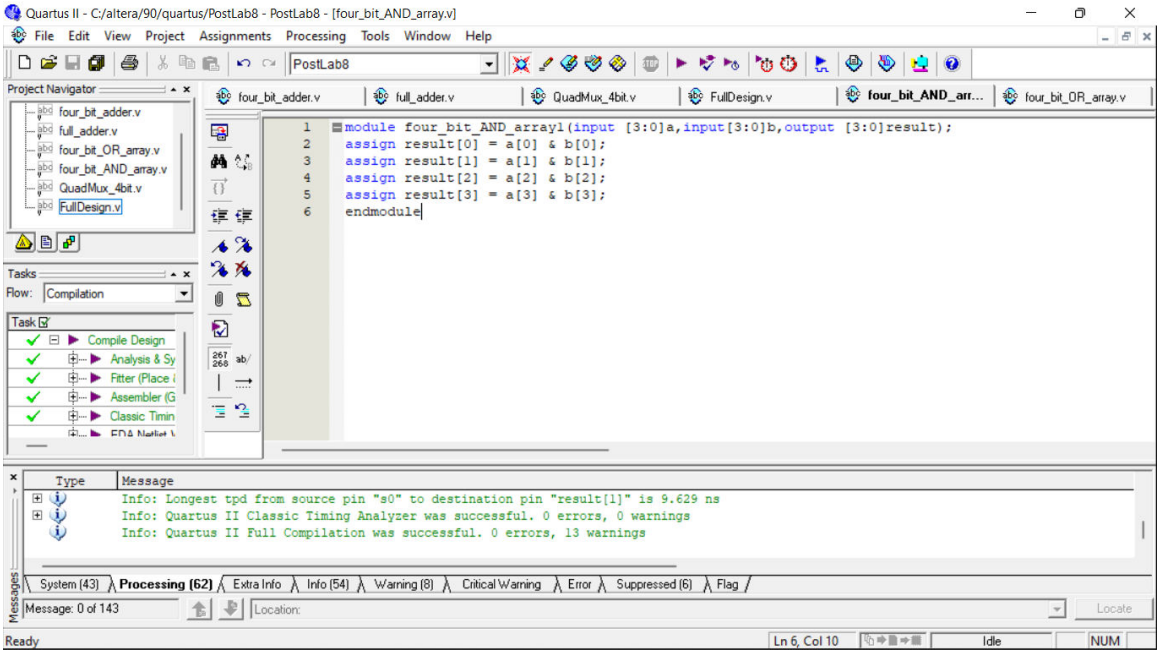
the question::

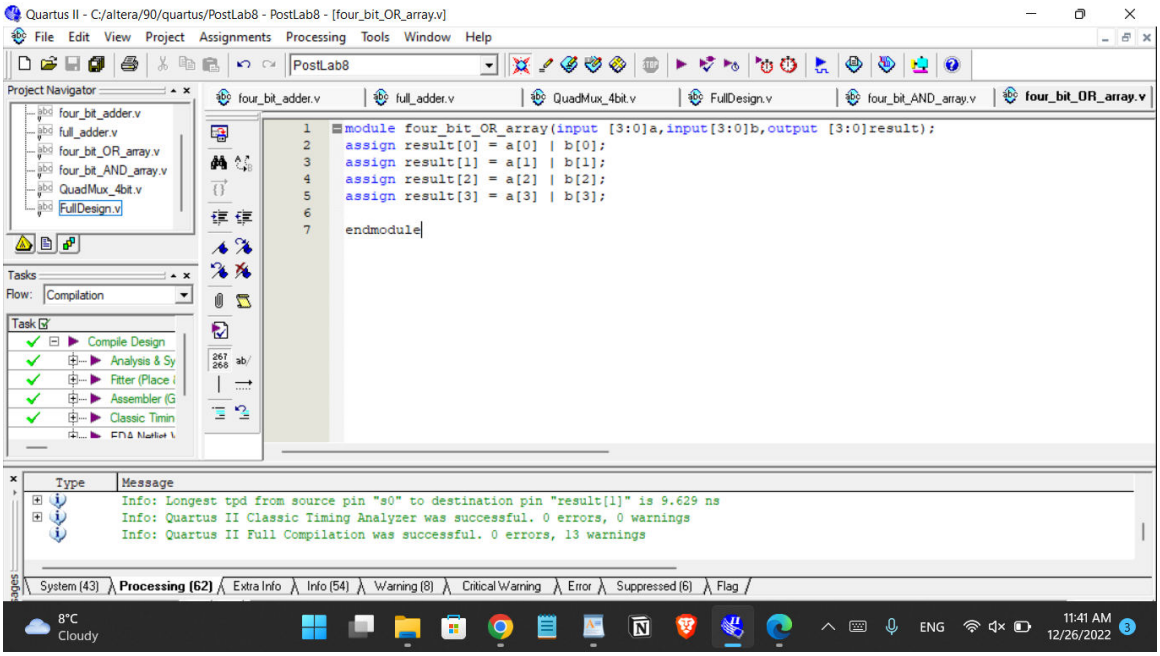


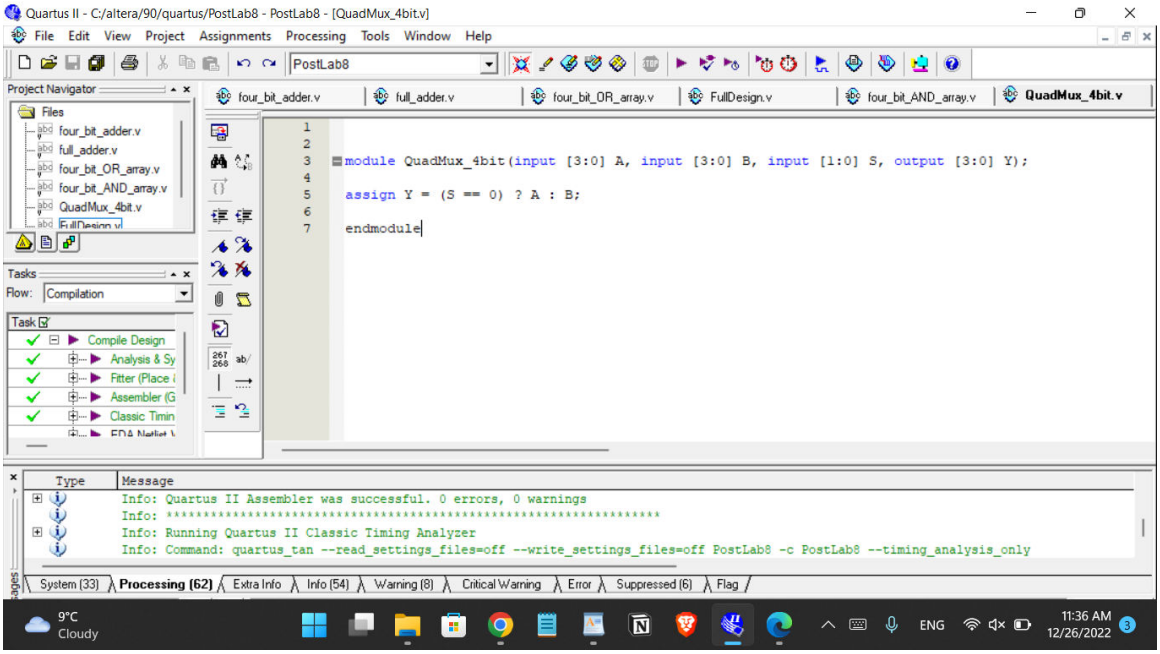
verilog code

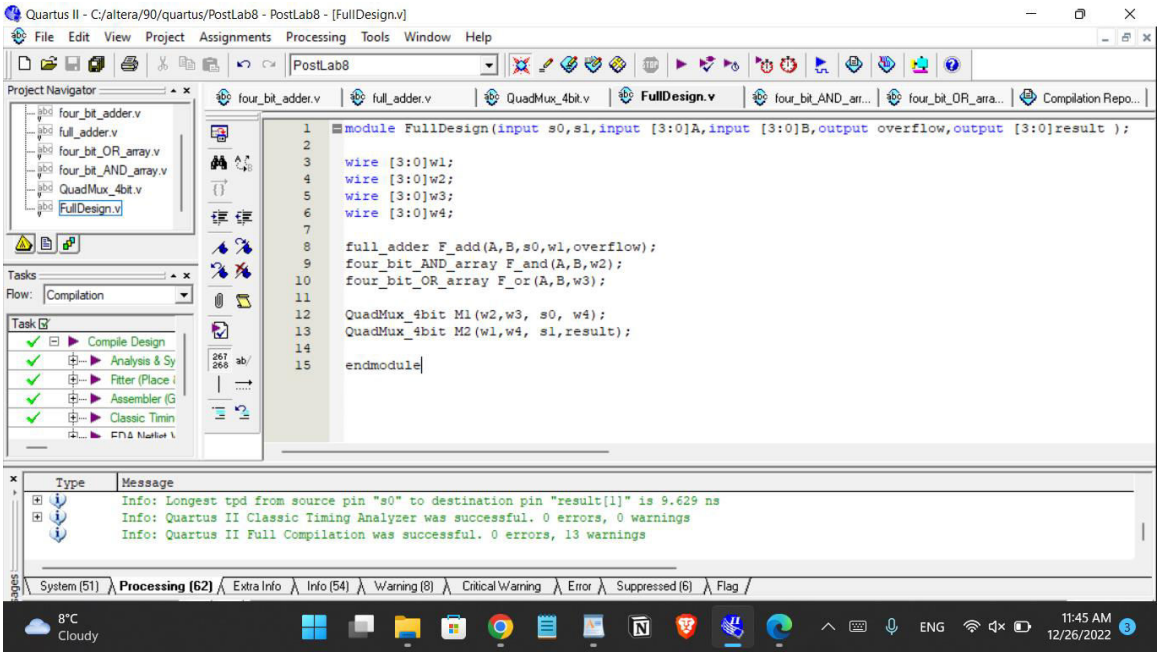



Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [full_adder.v]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
Project Navigator
full_adder.v
four_bit_OR_array.v
four_bit_AND_array.v
QuadMux_4bit.v
FullDesign.v
four_bit_adder.v
full_adder.v
four_bit_OR_arra...
four_bit_OR_arra...
four_bit_AND_arr...
QuadMux_4bit.v*
FullDesign.v
1 module full_adder(input a,b,c,output sum,cout);
2
3 assign sum=a^b^c;
4 assign cout=(a&b)||(b&c)||(a&c);
5 endmodule
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Sy
Fitter (Place
Assembler (G
Classic Timin
Type Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off PostLab8 -c PostLab8 --timing_analysis_only
System (33) Processing (62) Extra Info Info (54) Warning (8) Critical Warning Error Suppressed (6) Flag
9°C
Cloudy
ENG
11:33 AM
12/26/2022

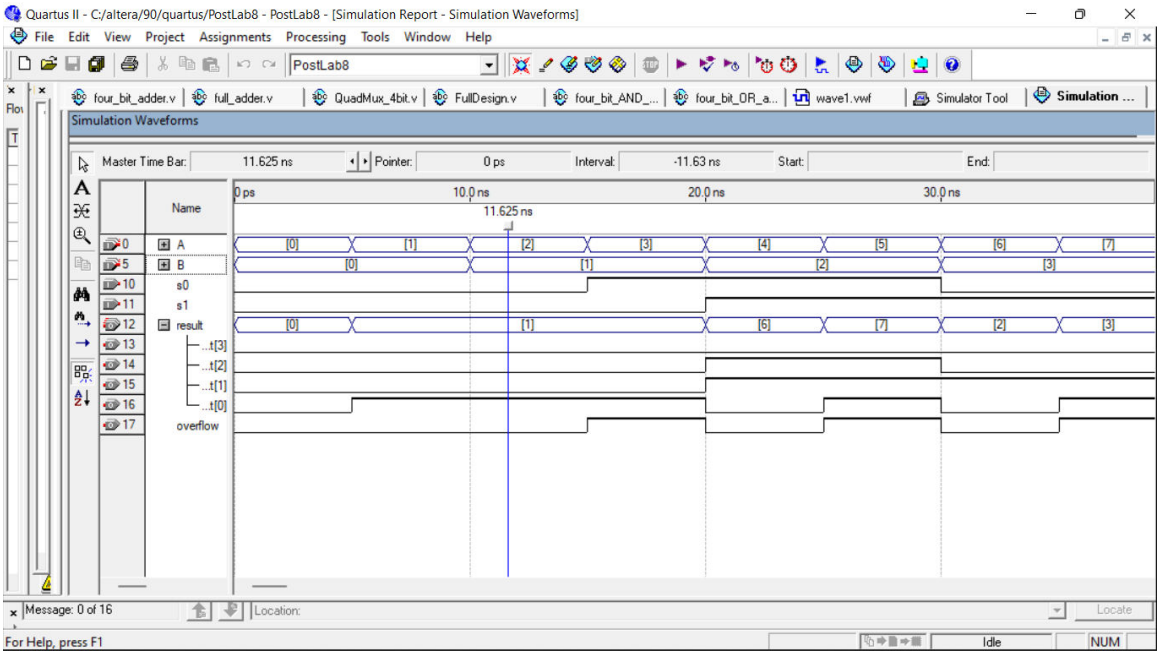

Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [four_bit_AND_array.v]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
Project Navigator
four_bit_adder.v
full_adder.v
four_bit_OR_array.v
four_bit_AND_array.v
QuadMux_4bit.v
FullDesign.v
four_bit_adder.v
full_adder.v
QuadMux_4bit.v
FullDesign.v
four_bit_AND_arr...
four_bit_OR_array.v
1 module four_bit_AND_array1(input [3:0]a,input[3:0]b,output [3:0]result);
2 assign result[0] = a[0] & b[0];
3 assign result[1] = a[1] & b[1];
4 assign result[2] = a[2] & b[2];
5 assign result[3] = a[3] & b[3];
6 endmodule
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Sy
Fitter (Place
Assembler (G
Classic Timin
Type Message
Info: Longest tpd from source pin "s0" to destination pin "result[1]" is 9.629 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 13 warnings
System (43) Processing (62) Extra Info Info (54) Warning (8) Critical Warning Error Suppressed (6) Flag
Message: 0 of 143
Location:
Locate
Ready
Ln 6, Col 10
Idle
NUM


Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [four_bit_OR_array.v]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
Project Navigator
four_bit_adder.v
full_adder.v
four_bit_OR_array.v
four_bit_AND_array.v
QuadMux_4bit.v
FullDesign.v
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Sy
Fitter (Place
Assembler (G
Classic Timin
1 module four_bit_OR_array(input [3:0]a,input[3:0]b,output [3:0]result);
2 assign result[0] = a[0] | b[0];
3 assign result[1] = a[1] | b[1];
4 assign result[2] = a[2] | b[2];
5 assign result[3] = a[3] | b[3];
6
7 endmodule
Type
Message
Info: Longest tpd from source pin "s0" to destination pin "result[1]" is 9.629 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 13 warnings
System (43) Processing (62) Extra Info Info (54) Warning (8) Critical Warning Error Suppressed (6) Flag
8°C
Cloudy
ENG
11:41 AM
12/26/2022

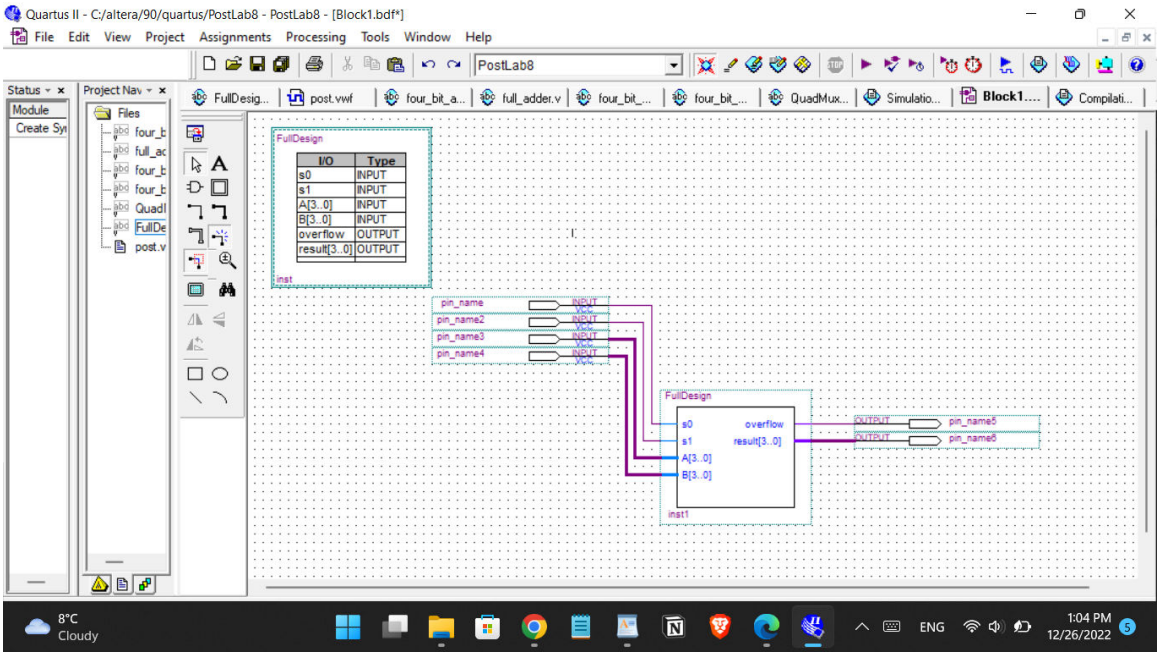

Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [QuadMux_4bit.v]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
Project Navigator
Files
four_bit_adder.v
full_adder.v
four_bit_OR_array.v
four_bit_AND_array.v
QuadMux_4bit.v
FullDesign.v
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Sy
Fitter (Place
Assembler (G
Classic Timin
1
2
3 module QuadMux_4bit(input [3:0] A, input [3:0] B, input [1:0] S, output [3:0] Y);
4
5 assign Y = (S == 0) ? A : B;
6
7 endmodule
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off PostLab8 -c PostLab8 --timing_analysis_only
System (33) Processing (62) Extra Info Info (54) Warning (8) Critical Warning Error Suppressed (6) Flag
9°C
Cloudy
ENG
11:36 AM
12/26/2022



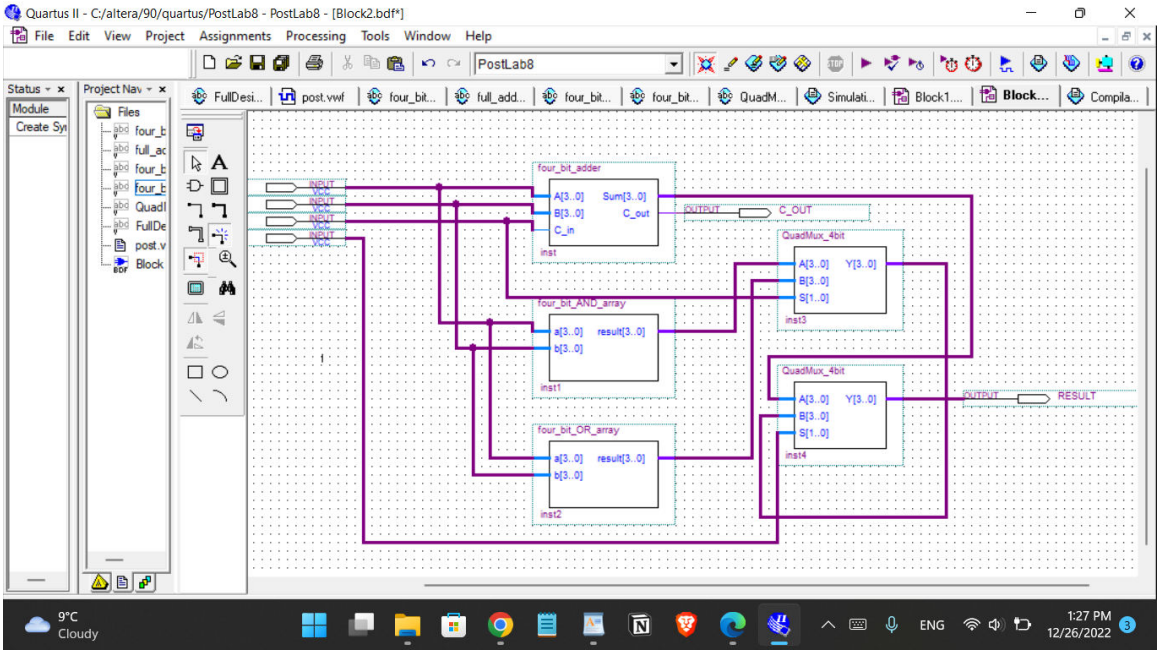
waveform::



Block Diagram::


Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [Block1.bdf*]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
FullDesign
I/O Type
s0 INPUT
s1 INPUT
A[3..0] INPUT
B[3..0] INPUT
overflow OUTPUT
result[3..0] OUTPUT
pin_name
pin_name2
pin_name3
pin_name4
pin_name5
pin_name6
inst1
8°C Cloudy
ENG
1:04 PM
12/26/2022

or


Quartus II - C:/altera/90/quartus/PostLab8 - PostLab8 - [Block2.bdf*]
File Edit View Project Assignments Processing Tools Window Help
PostLab8
four_bit_adder
four_bit_AND_array
four_bit_OR_array
QuadMux_4bit
C_OUT
RESULT
9°C Cloudy
ENG
1:27 PM
12/26/2022