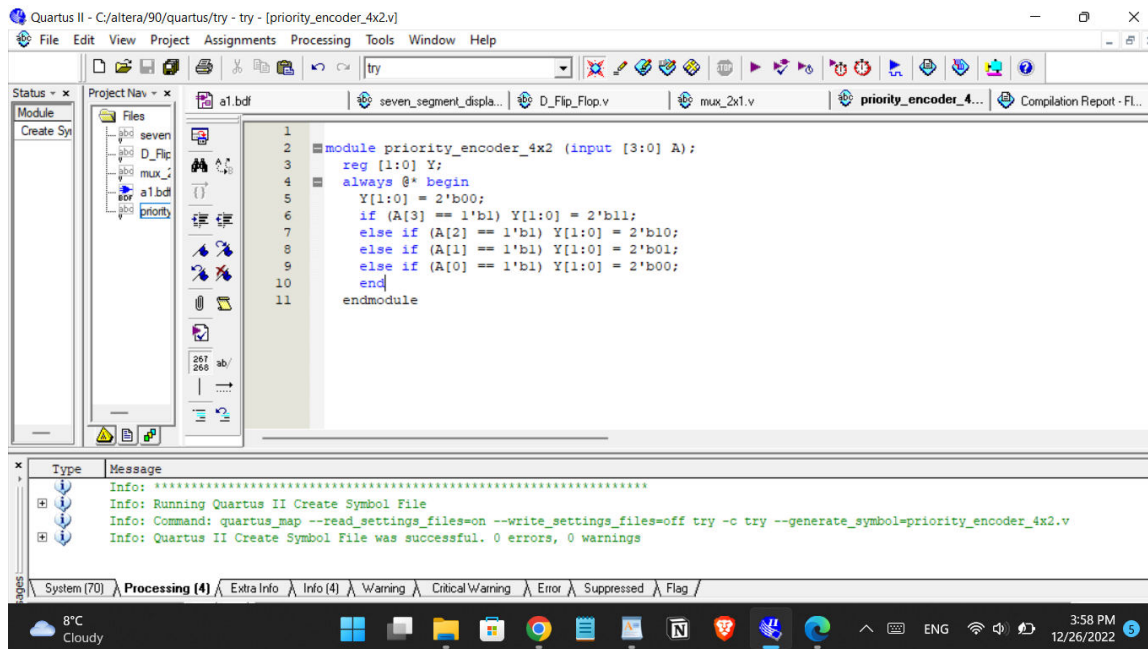


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Std.no::1210084

preLab9





```
module priority_encoder_4x2 (input [3:0] A);
```

```
    reg [1:0] Y;
```

```
    always @* begin
```

```
        Y[1:0] = 2'b00;
```

```
        if (A[3] == 1'b1) Y[1:0] = 2'b11;
```

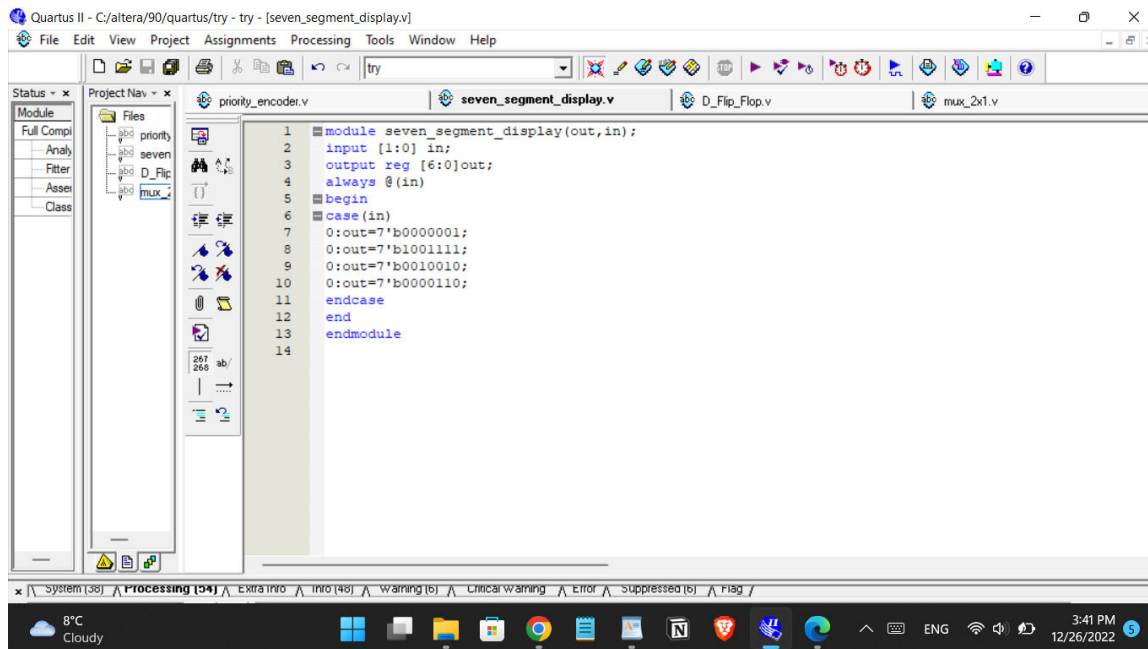
```
        else if (A[2] == 1'b1) Y[1:0] = 2'b10;
```

```
        else if (A[1] == 1'b1) Y[1:0] = 2'b01;
```

```
        else if (A[0] == 1'b1) Y[1:0] = 2'b00;
```

```
    end
```

```
endmodule
```



```
module seven_segment_display(out,in);
```

```
input [1:0] in;
```

```
output reg [6:0]out;
```

```
always @(in)
```

```
begin
```

```
case(in)
```

```
0:out=7'b0000001;
```

```
0:out=7'b1001111;
```

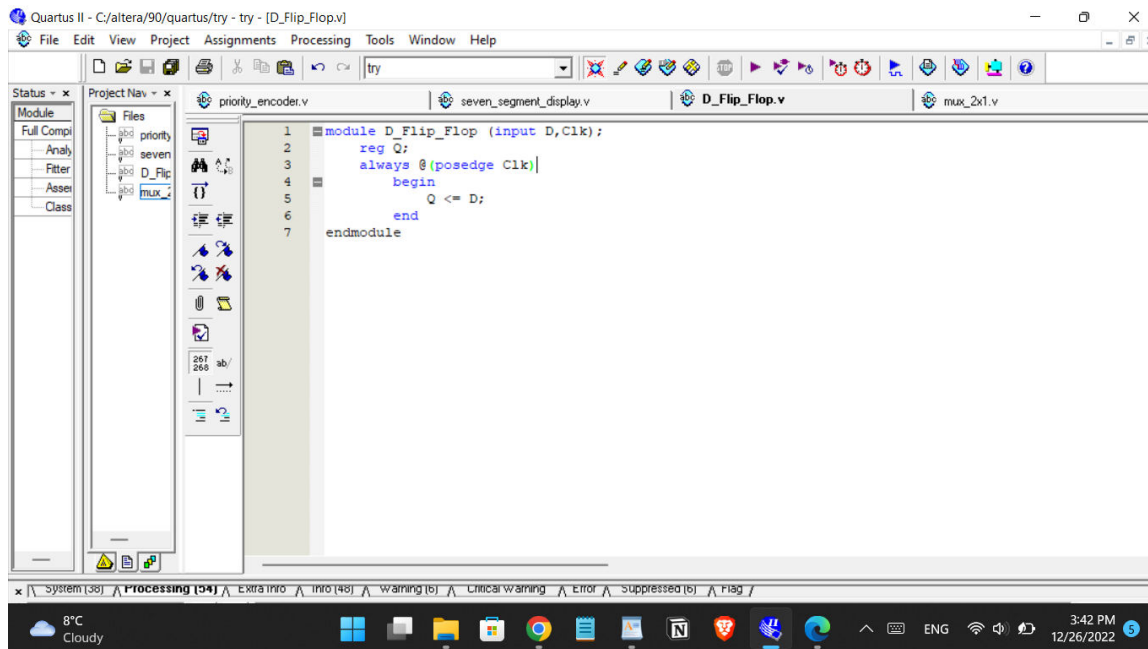
```
0:out=7'b0010010;
```

```
0:out=7'b0000110;
```

```
endcase
```

```
end
```

```
endmodule
```



```
module D_Flip_Flop (input D,Clk);
```

```
    reg Q;
```

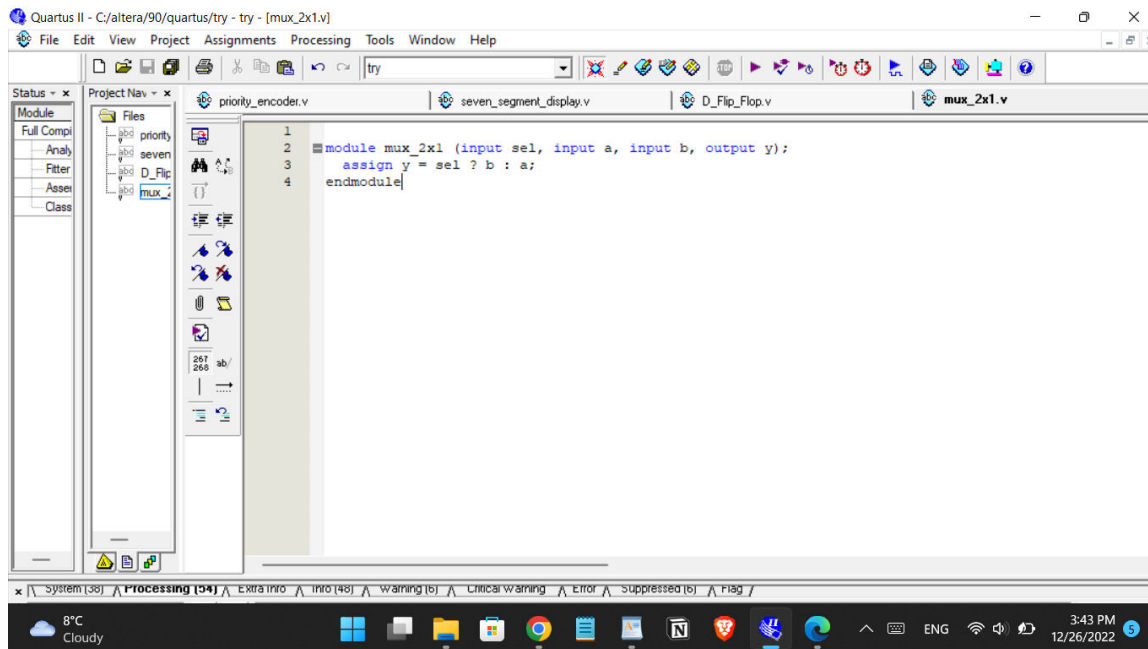
```
    always @(posedge Clk)
```

```
        begin
```

```
            Q <= D;
```

```
        end
```

```
endmodule
```



```
module mux_2x1 (input sel, input a, input b, output y);
```

```
    assign y = sel ? b : a;
```

```
endmodule
```