Faculty of Engineering and Technology – Electrical and Computer Engineering Department

Verilog Todo

Given the following Combinational circuit, Use Verilog HDL on Quartus tool to

a. Implement the 1-bit adder and use it to build 4-bit adder structurally
b. Implement the MUX2x1 using behavioral and then use it to build the Quad MUX 2x1 structurally.
c. Implement the 4-bit OR Array using Data flow
d. Implement the 4-bit AND Array structurally
e. Use the blocks you implemented in the parts above to build the final system shown in the figure.
f. You should show simulation results for each of the above parts