Birzeit University
Faculty of Engineering and Technology
Electrical and Computer Engineering Department
Digital Systems ENCS2340
Verilog HDL Project

Project: 1-bit simple ALU

Due Thursday, August 25, 2022

This project is to be done individually:

1) You need to submit your codes.

2) Write a report for your results by providing the code and the simulation results (testing) of every component as well as the whole system.

In this project, you need to implement 1-bit ALU circuit shown in Figure below. You need to build the system components (Muxs and adder) separately using Verilog HDL. Then, you have to integrate the different system components to build the whole system. Each of the system components, as well as, the whole system should be verified using simulation. **Also, you need to drive the functionality of the circuit (using truth table) when changing the control inputs (invert A, invert B, Carry in, and Operation).**